- **10-Gbps Ethernet LAN PCS With 64b/66b ENDEC**
- **10-Gbps Media-Independent Interface (XGMII) Using 2.5-V SSTL Class 2 Technology**
- **10-Gbps 16-Bit Interface (XSBI) Using LVDS Technology**
- **IEEE 802.3 Management Data Interface (MDIO)**
- **Advanced 0.18-μm CMOS Technology**
- **Less Than 1.5 W Power Consumption**
- **Low-Cost 289-Ball PBGA Package**

description

The DLKPC192S performs all physical coding sublayer (PCS) functions for proposed IEEE 802.3ae/D2.0 10-Gbps Ethernet serial network (LAN) connections.

The DLKPC192S connects to the media access control (MAC) and all higher layers of the OSI protocol stack via the 10-Gbps media independent interface (XGMII). The XGMII consists of two unidirectional buses, each with 36 information bits (32 data bits, 4 control bits) plus a clock. The XGMII interface is implemented using 2.5-V, SSTL Class 2 technology. The DLKPC192S connects to physical media via the 10-Gbps 16-bit interface (XSBI). The XSBI bus consists of two unidirectional buses, each with 16 data bits plus a clock. The XSBI interface is implemented utilizing low-voltage differential signaling (LVDS) technology. The DLKPC192S encodes and decodes data using the 64b/66b coding algorithm and provides clock tolerance compensation when needed.

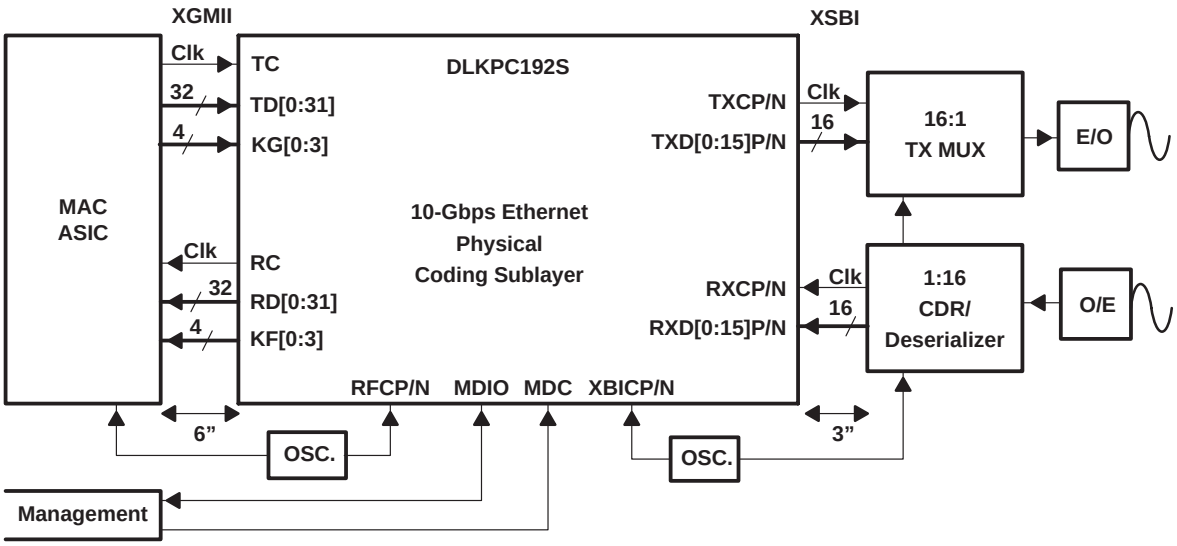


Figure 1. 10-Gbps Ethernet Short-PCB-Distance Implementation

The DLKPC192S can be used in systems where printed-circuit board (PCB) traces between the media access control device and the serializer/deserializer device are sufficiently short, as shown in Figure 1.

Systems requiring PCB traces longer than 6 inches can be implemented by using the TLK3114SA XGMII external sublayer device to increase the allowable PCB trace length to greater than 20 inches, as shown in Figure 2.

description (continued)

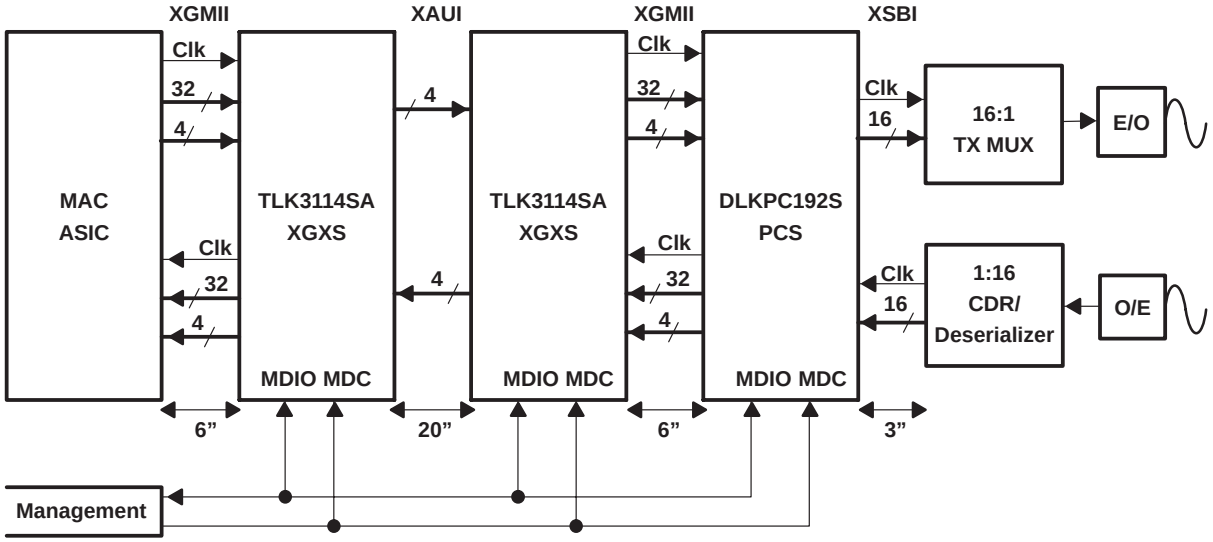


Figure 2. 10-Gbps Ethernet Long-PCB-Distance Implementation

The DLKPC192S supports the IEEE 802.3 defined management interface (MDIO) to allow ease in configuration and status monitoring of the link.

The DLKPC192S is implemented in 0.18-µm CMOS technology. The DLKPC192S operates with core and I/O supplies of 1.8 V, 2.5 V, and 3.3 V while dissipating less than 1.5 W. The device is packaged in a 19×19-mm, 289-terminal plastic ball grid array (PBGA) package and is characterized for operation from 0°C to 70°C.

Figure 3 is a high-level block diagram of the DLKPC192S. The basic operation of the DLKPC192S is described in the following paragraphs, with the transmit path being described first, followed by the receive path.

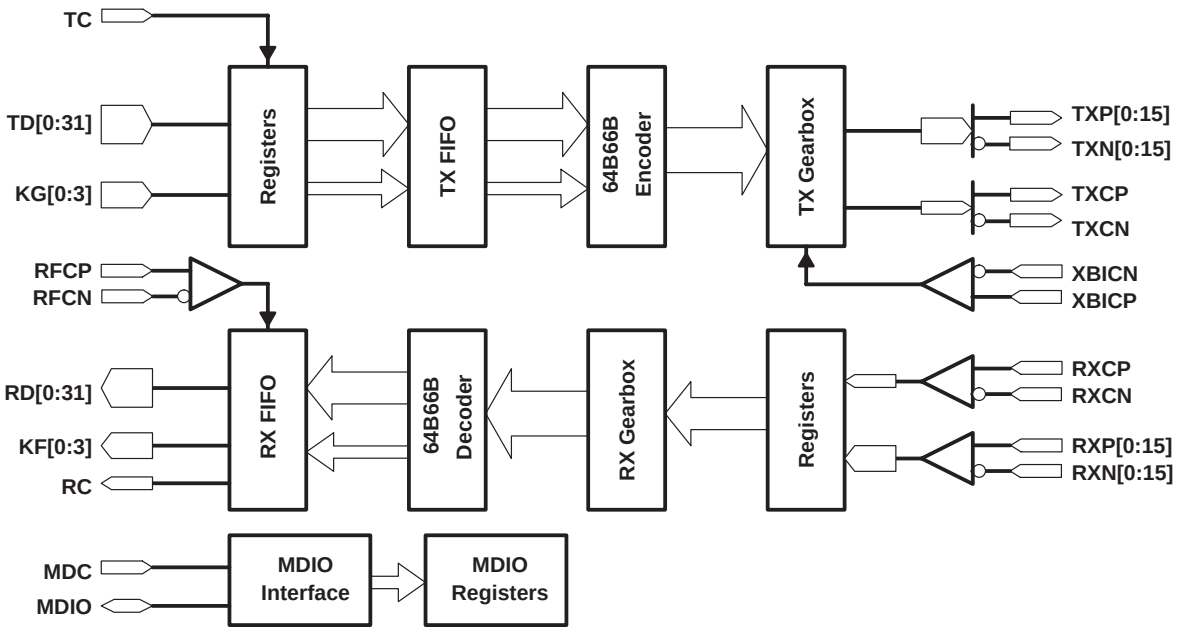


Figure 3. The DLKPC192S Block Diagram

terminal locations (top view)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	
17	DVAD [1]	DVAD [0]	GND	TXP [0]	TXP [1]	GND	TXP [4]	TXCP	VDDS	VDD	TXP [10]	GND	GND	TXN [15]	GND	XBIOR _IREF	MDIO	17
16	DVAD [2]	VDDO	VDD	TXN[0]	TXN[1]	VDDS	TXN[4]	TXCN	TXP[7]	GND	TXN [10]	TXP [11]	VDDS	TXP [15]	VDD	XBIOR _VREF	MDC	16
15	DVAD [3]	DVAD [4]	GND	GND	VDD	GND	VDD	GND	TXN[7]	TXP[8]	GND	TXN [11]	TXP [13]	TXP [14]	GND	VDD	GND	15
14	TD[2]	TD[1]	TD[0]	TD[3]	TXN[2]	TXP[2]	VDDS	TXP[5]	TXP[6]	TXN[8]	TXP[9]	TXN [12]	TXN [13]	TXN [14]	AKR_ NI	XBICP	XBICN	14
13	TD[5]	GND	TD[6]	VDD	TD[4]	TXN[3]	TXP[3]	TXN[5]	TXN[6]	VDDS	TXN[9]	TXP [12]	VDDS	RXN [0]	RXP[0]	RXN[1]	RXP[1]	13
12	TD[9]	TD[10]	TD[8]	TD[7]	TD[11]	GND	GND	GND	GND	GND	GND	GND	RXN[2]	RXP[2]	VDDS	RXN[3]	RXP[3]	12
11	GND	VDD	GND	VDDO	TD[12]	GND	GND	GND	GND	GND	GND	GND	RXN[4]	RXP[4]	GND	RFCP	RFCN	11
10	TD[16]	TD[17]	TD[15]	TD[14]	TD[13]	GND	GND	GND	GND	GND	GND	GND	RXN [6]	VDDS	RXN [5]	RXP [5]	GND	10
9	VDDO	TD[19]	TD[20]	TD[18]	TC	GND	GND	GND	GND	GND	GND	GND	RXP[6]	VDD	RXN [7]	RXP [7]	GND	9
8	GND	VDD	GND	VDDO	TD[21]	GND	GND	GND	GND	GND	GND	GND	RXN [8]	RXP[8]	VDDS	RXP [9]	RXN [9]	8
7	TD[25]	TD[24]	TD[23]	TD[26]	TD[22]	GND	GND	GND	GND	GND	GND	GND	RXN [10]	RXP [10]	GND	RXCN	RXCP	7
6	TD[29]	GND	TD[28]	VDD	TD[27]	GND	GND	GND	GND	GND	GND	GND	RXN [11]	RXP [11]	VDDS	RXN [12]	GND	6
5	KG[0]	TD[31]	TD[30]	KG[1]	RD[5]	RD[8]	RD[11]	RD[15]	RC	RD[20]	RD[25]	RD[30]	RXP [13]	RXN [13]	VDDS	RXP [12]	GND	5
4	KG[3]	KG[2]	GND	GND	RD[6]	VDDO	RD[12]	RD[16]	VDDO	RD[21]	RD[26]	VDDO	RD[31]	RXP [15]	RXN [15]	RXP [14]	RXN [14]	4
3	SSTL _REF	VDDO	VDD	RD[2]	RD[7]	GND	RD[13]	RD[17]	GND	RD[22]	RD[27]	GND	KF[2]	VDD	XBIIR _IREF	XBIIR _VREF	GND	3
2	GND	GND	RD[0]	RD[3]	VDDO	RD[9]	VDD	VDDO	RD[18]	RD[24]	VDDO	RD[28]	KF[1]	VDDO	GND	VDD	TEST	2
1	GND	VDDO	RD[1]	RD[4]	GND	RD[10]	RD[14]	GND	RD[19]	RD[23]	GND	RD[29]	KF[0]	KF[3]	SSTL MODE	GND	RSTN	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	

Signal Terminal Functions

XGMII interface terminals

SIGNAL	LOCATION	TYPE	DESCRIPTION
TC	E9	SSTL class 2, 2.5-V input	XGMII transmit clock. The XGMII transmit data on TD[0:31] and control word generator signals on KG[0:3] are latched on the rising and falling edges of TC.
TD[0:31]	C14, B14, A14, D14, E13, A13, C13, D12, C12, A12, B12, E12, E11, E10, D10, C10, A10, B10, D9, B9, C9, E8, E7, C7, B7, A7, D7, E6, C6, A6, C5, B5	SSTL class 2, 2.5-V input	XGMII transmit data. The data on this bus is latched on the rising and falling edges of TC.
KG[0:3]	A5, D5, B4, A4	SSTL class 2, 2.5-V input	XGMII transmit control word. The control signals on these terminals are used to designate whether the data on the TD bus is data characters or protocol control characters. When high, these terminals cause the data on corresponding byte of the TD bus to be interpreted as control characters by the PCS. The assignment of control bits on this bus to corresponding bytes of the TD bus is as follows: KG0 − TD[0:7] KG1 − TD[8:15] KG2 − TD[16:23] KG3 − TD[24:31] The value of these signals is latched on the rising and falling edge of TC.
RC	J5	SSTL class 2, 2.5-V output	XGMII receive clock. The received data and the control word generator signals are transferred across the XGMII bus on RD[0:31] and KF[0:3], respectively, on the rising and falling edges of RC. RC is generated from the input reference clock RFCP/RFCN.
RD[0:31]	C2, C1, D3, D2, D1, E5, E4, E3, F5, F2, F1, G5, G4, G3, G1, H5, H4, H3, J2, J1, K5, K4, K3, K1, K2, L5, L4, L3, M2, M1, M5, N4	SSTL class 2, 2.5-V output	XGMII receive data. Parallel data on this bus is output on the rising and falling edges of RC.
KF[0:3]	N1, N2, N3, P1	SSTL class 2, 2.5-V output	XGMII receive control word. The control signals on these terminals are used to designate whether the data on the RD bus is data characters or protocol control characters. When high, these terminals indicate the data on corresponding byte of the RD bus is protocol control characters. The assignment of control bits on this bus to corresponding bytes of the RD bus is as follows: KF0 − RD[0:7] KF1 − RD[8:15] KF2 − RD[16:23] KF3 − RD[24:31] Data on these terminals is valid on the rising and falling edges of RC.

Signal Terminal Functions (Continued)

XSBI interface terminals

SIGNAL	LOCATION	TYPE	DESCRIPTION
TXCP/TXCN	H17, H16	LVDS output	XSBI transmit clock. Differential output clock. The data on TXP[0:15]/TXN[0:15] is transferred on the rising edge of the transmit data clock. Nominal frequency of TXCP/TXCN is 644.53125 MHz.
TX[0:15]P/N	D17, D16, E17, E16, F14, E14, G13, F13, G17, G16, H14, H13, J14, J13, J16, J15, K15, K14, L14, L13, L17, L16, M16, M15, M13, M14, N15, N14, P15, P14, P16, P17	LVDS output	XSBI transmit data. Parallel data on this bus is clocked on the rising edge of TXCP.
RXCP/RXCN	U7, T7	LVDS input	XSBI receive clock. Differential input clock. The data on RXP[0:15]/RXN[0:15] is latched on the rising edge of this clock. Please note, the positive side of this differential clock (RXCP) needs to rise *in the middle of the data*. Nominal frequency of RXCP/RXCN is 644.53125 MHz. There is a 100-Ω on-chip termination resistor placed differentially between the terminals of each terminal pair.
RX[0:15]P/N	R13, P13, U13, T13, P12, N12, U12, T12, P11, N11, T10, R10, N9, N10, T9, R9, P8, N8, T8, U8, P7, N7, P6, N6, T5, T6, N5, P5, T4, U4, P4, R4	LVDS input	XSBI receive data. Parallel data on this bus is valid on the rising edge of RXCP/RXCN. There is a 100-Ω on-chip termination resistor placed differentially between the terminals of each terminal pair.

management data interface

SIGNAL	LOCATION	TYPE	DESCRIPTION
MDIO	U17	LVTTL input/output	Management data input/output. MDIO is the bidirectional serial data path for the transfer of management data to and from the DLKPC192S device.
MDC	U16	LVTTL input	Management data clock. MDC is the clock for the transfer of management data to and from the protocol device.
DVAD[0:4]	B17, A17, A16, A15, B15	LVTTL input	Management address. These terminals determine the device address on the MDIO interface to which the DLKPC192S responds. The DLKPC192S only responds to valid commands that contain a device address equal to the value seen on these terminals.

reference clock terminals

SIGNAL	LOCATION	TYPE	DESCRIPTION
RFCP/RFCN	T11, U11	LVDS input	XGMII receive reference clock. Differential reference clock for generation of XGMII receive interface functions. Nominal frequency of RFCP/RFCN is 156.25 MHz. There is a 100-Ω on-chip termination resistor placed differentially between the two terminals.
XBICP/XBICN	T14, U14	LVDS input	XSBI transmit reference clock. Differential reference clock for generation of XSBI transmit interface functions. Nominal frequency of XBICP/XBICN is 644.53125 MHz. There is a 100-Ω on-chip termination resistor placed differentially between the two terminals

Signal Terminal Functions (Continued)

miscellaneous terminals

SIGNAL	LOCATION	TYPE	DESCRIPTION
RSTN	U1	LVTTL input (with pullup)	Chip reset. Low-true device reset. When low, the DLKPC192S is held in a reset state.
TEST	U2	LVTTL input (with pullup)	Test. When this terminal is held high, the device is placed in test mode. This terminal is used for device test during manufacturing. Some terminals of the device may change functionality while TEST is high. The use of this terminal is reserved for Texas Instruments and may provide for capabilities such as IDDQ testing. When TEST is low the device operates normally.
AKR_NI	R14	LVTTL input	XGMII IPG mode. Controls the behavior of the transmit and receive FIFO circuits on the XGMII input and output interface. See section on IPG modes.

voltage supply and reference terminals

SIGNAL	LOCATION	TYPE	DESCRIPTION
SSTL_REF	A3	Input	SSTL input voltage reference. 1.25 V relative to VSS
XBIOR_IREF	T17	Input	LVDS reference current for LVDS drivers. 1 kΩ to VSS
XBIOR_VREF	T16	Input	LVDS reference voltage for LVDS drivers. 1.2 V relative to VSS
XBIIR_IREF	R3	Input	LVDS reference current for LVDS receivers. 1 kΩ to VSS
XBIIR_VREF	T3	Input	LVDS reference voltage for LVDS receivers. 1.2 V relative to VSS
SSTL_MODE	R1	LVTTL input	Mode control for SSTL output buffers. A low value sets the output drivers in SSTL-2 mode, while a high value sets the outputs to SSTL-1 mode.
VDD	C3, G2, P3, T2, P9, T15, C16, E15, G15, K17, R16, D6, B8, B11, D13	Supply	1.8 V. Provides power for core and I/O cells requiring it
VDDS	R5, R6, R8, P10, R12 F16, G14, J17, K13, N16, N13	Supply	3.3 V. Provides power for all LVDS and LVTTL I/Os
VDDO	B1, E2, J4, M4, P2, F4, H2, L2, B3, A9, B16, D8, D11	Supply	2.5 V. Provides power for all SSTL I/Os
VSS	A1, B2, D4, E1, F3, H1, J3, L1, M3, R2, T1, U3, U5, U6, R7, U9, U10, R11, U15, C17, D15, F17, F15, H15, K16, L15, M17, N17, R17, R15, A2, C4, B6, A8, C8, A11, C11, B13, C15	Ground	Ground. Return for all supplies

thermal ground terminals

SIGNAL	LOCATION	TYPE	DESCRIPTION
T-GND	F6, G6, H6, J6, K6, L6, M6, F7, G7, H7, J7, K7, L7, M7, F8, G8, H8, J8, K8, L8, M8, F9, G9, H9, J9, K9, L9, M9, F10, G10, H10, J10, K10, L10, M10, F11, G11, H11, J11, K11, L11, M11, F12, G12, H12, J12, K12, L12, M12		Thermal ground connections

detailed description

transmission

The DLKPC192S accepts data with appropriate control coding on the 10-Gbps media-independent interface (XGMII) as defined in the proposed IEEE P802.3ae standard. Data to be transmitted is clocked from the XGMII interface into a register bank. The data is then transferred into the transmission FIFO. Data is pulled from the FIFO, encoded via the 64b/66b encoder, and then disassembled into 16-bit words by the transmission gearbox and transferred out over the XSBI interface.

XGMII transmit data bus timing

From the XGMII, the DLKPC192S latches the data on transmit data bus TD[0:31] along with the associated byte level control terminals, KG[0:3]. Data is latched on both the rising and falling edges of the transmit data clock, TC, as the XGMII interface is defined as a double-data-rate (DDR) interface. The basic timing is shown in Figure 4. Detailed timing information is provided in the *XGMII* paragraph of the *timing—reference clock* section.

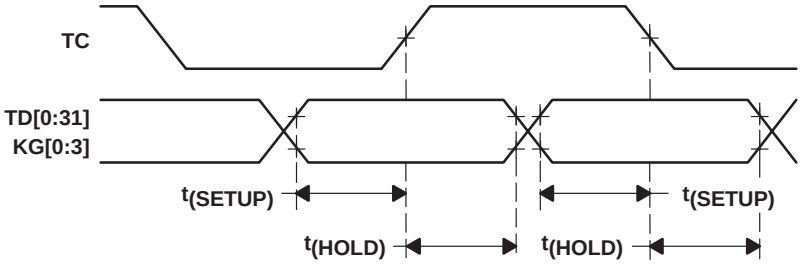


Figure 4. XGMII Transmit Timing

transmit FIFO

The transmit FIFO provides sufficient buffer to compensate for both short-term clock-phase jitter and long-term frequency differences between the input data rate at the XGMII interface to the output data rate at the XSBI interface. Logic within the transmit FIFO provides the ability for the insertion or deletion of characters when the transfer rate between the interfaces differs. If not for this ability, FIFO overruns or underruns could occur and cause corruption of data. The logic within the transmit FIFO performs inserts or deletes, when necessary, in such a way as to prevent corruption of Ethernet packets being transferred through the DLKPC192S.

64b/66b encode

To facilitate the transmission of data received from the media access control (MAC) layer, the DLKPC192S encodes data received from the MAC using the 64b/66b encoding algorithm defined in the proposed IEEE 802.3ae standard. The DLKPC192S takes two consecutive transfers from the XGMII interface and encodes them into a 66-bit code word. The information from the two XGMII transfers includes 64 bits of data and 8 bits of control information. Not all combinations of control and data information are valid and, if the 64b/66b encoder detects an invalid combination, the 64b/66b encoder replaces erroneous information with appropriately encoded error information. The resulting 66-bit code word is then sent on to the transmit gearbox.

The encoding process is fully described within the proposed IEEE 802.3ae standard. It includes two steps, an encoding step which converts the 72 bits of data received from the transmit FIFO block into a 66-bit code word and then a scrambling step which scrambles 64 bits of encoded data using the scrambling algorithm $x^{57}+x^{39}+1$. The 66 bits created by the encoder consists of 64 bits of data and a 2-bit synchronization field consisting of either 01 or 10. Only the 64 bits of data are scrambled, leaving the two synchronization bits unmodified. The two synchronization bits allow the receive gearbox to obtain frame alignment and, in addition, ensure an edge transition at least once in 66 bits of data. The encoding process allows a limited amount of control information to be sent in-line with the data.

transmission (continued)

transmit gearbox

The function of the transmit gearbox is to convert the 66-bit encoded data stream coming out of the 64b/66b encoder into a 16-bit-wide data stream to be sent out on the XSBI bus to the physical media attachment (PMA) device. While the effective bit rate of the 66 bit data stream is equal to the effective bit rate of the 16-bit XSBI bus, the clock rates of the two buses are of different frequencies, thus the need for the gearbox.

XSBI transmit data bus

The connection to the PMA is via a 16-bit wide LVDS parallel data bus. Data is placed on the TXP[0:15]/ TXN[0:15] terminals. The LVDS clock on TXCP/TXCN clocks the data. Data is valid on the falling edge of TXC. The data and clock signals are aligned as shown in Figure 5. A differential reference clock input is used as the clock source to generate the output timing. The reference input clock is provided on XBICP/XBICN terminals. A 100-Ω on-chip termination resistor is placed differentially at the LVDS input pair for the reference clock.

Detailed timing information is provided later in the *XSBI* paragraph of the *timing—reference clock* section.

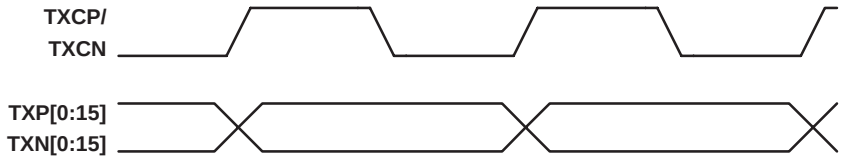


Figure 5. XSBI Transmit Output Timing Waveform

transmission latency

The data transmission latency of the DLKPC192S is defined as the delay from the edge of the XGMII transmit clock when valid data is latched on the XGMII to the rising edge of the XSBI transmit clock, TXP/TXN, when the last bit of the same data is output on the XSBI interface. The latency ($T_{LATENCY}$) is measured in TXC clock periods. The maximum latency is 99 TXC clock periods. If the latency is not an exact multiple of TXC clock periods, then the latency value is rounded down to the next lower number of TXC clock periods for the minimum latency and rounded up to the next higher integer number of TXC clock periods for the maximum latency.

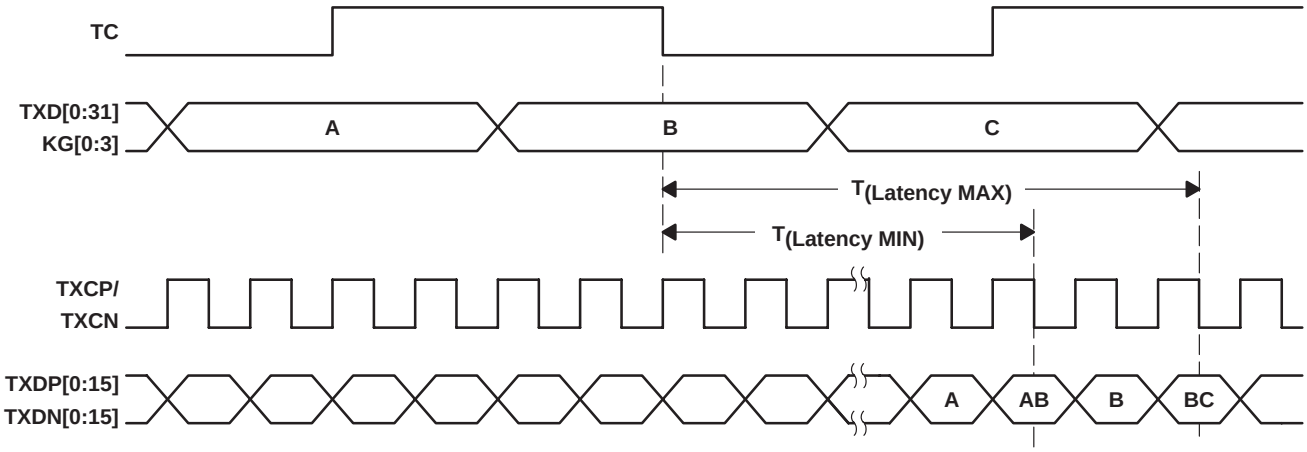


Figure 6. Transmitter Latency

reception

XSBI receive data bus

Connection from the PMA to the DLKPC192S is via a 16-bit-wide LVDS parallel bus. Data is received on the RXP[0:15]/RXN[0:15] terminals and is clocked in using the RXCP/RXCN clock. A 100-Ω on-chip termination resistor is placed differentially at each LVDS input pair. The rising edge of RXCP/RSCN is used to latch the data as shown in Figure 7. Please note, the phase relationship is such that the positive side of the differential clock needs to rise *in the middle of the data.* This is in contrast to the transmit XSBI interface. At that interface, the positive side of the clock is in phase with the data. To successfully loop the transmit path to the receive path of this PCS device you must attach TXCP to RXCN and TXCN to RXCP. Detailed timing information is provided later in the *XSBI* paragraph of the *timing—reference clock* section.

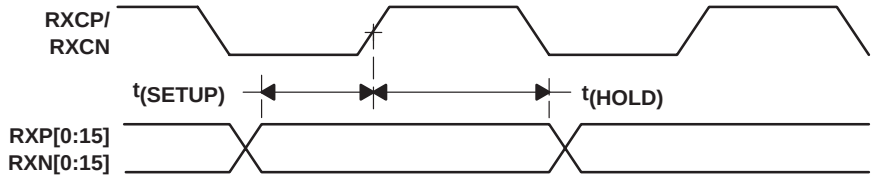


Figure 7. XSBI Receive Input Timing Waveform

receive gearbox

While the transmit gearbox only performs the task of converting 66-bit data to be transported on the 16-bit XSBI bus, the receive gearbox has more to do than just the reverse of this function. The receive gearbox must also determine where within the incoming data stream the boundaries of the 66-bit code words are. The receive gearbox has the responsibility of initially synchronizing the header field of the code words and continuously monitoring the ongoing synchronization. After obtaining synchronization to the incoming data stream, the gearbox assembles 66-bit code words and presents these to the 66b/64b decoder. While the effective bit rate of the 66-bit data stream is equal to the effective bit rate of the 16-bit XSBI bus, the clock rates of the two buses are of different frequencies, thus the need for the gearbox.

66b/64b decode

The data received from the XSBI bus is encoded data. The DLKPC192S decodes the data received using the 66b/64b decoding algorithm defined in the proposed IEEE 802.3ae standard. The DLKPC192S creates consecutive 36-bit data words from the encoded 66-bit code words for transfer over the XGMII interface to the MAC. The information for the two XGMII transfers includes 64 bits of data and 8 bits of control information. Not all code words are valid. Invalid code words are handled by the 66b/64b decode block and appropriate error handling is provided, as defined in the proposed IEEE 802.3ae standard.

The decoding algorithm is fully described within the proposed IEEE 802.3ae standard. It includes two steps, a descrambling step which unscrambles 64 bits of the 66-bit code word, and a decoding step which converts the 66 bits of data received to two sets of data, each consisting of 32 bits of data and 4 bits of control information. These words are sent to the receive FIFO block. The descrambler reverses the scrambling algorithm $x^{57}+x^{39}+1$.

receive FIFO

The receive FIFO provides sufficient buffer to compensate for both short-term clock-phase jitter and long-term frequency differences between the input of data from the XSBI interface and the output of data over the XGMII interface. Logic within the receive FIFO provides the ability for the insertion or deletion of characters when the transfer rate between the interfaces differs. If not for this ability, FIFO overruns or underruns could occur and cause corruption of data. The logic within the receive FIFO performs inserts or deletes, when necessary, in such a way as to prevent corruption of Ethernet packets being transferred through the DLKPC192S.

XGMII receive data bus timing

The receiver portion of the XGMII interface on the DLKPC192S outputs the decoded data on RD[0:31] and byte control flags, KF[0:3]. The XGMII interface is a DDR interface, so data is transferred on both the rising and falling edges of the XGMII receive data clock, RC. The basic timing is shown in Figure 8. Detailed timing information is provided later in this document.

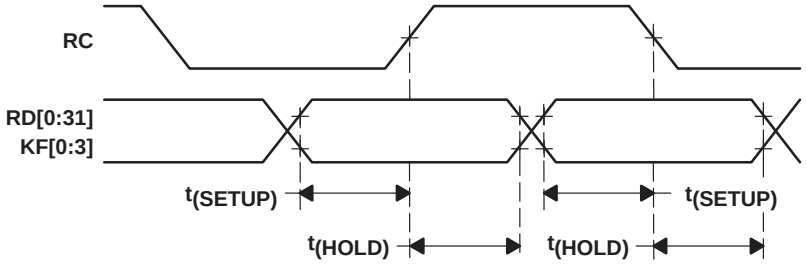


Figure 8. Receive Interface Timing

data reception latency

The data reception latency of the DLKPC192S is defined as the delay from the edge of the XSBI transmit clock when valid data is latched on the XSBI to the rising edge of the XGMII transmit clock, RC, when the last bit of the same data is output on the XGMII interface. The latency ($R_{LATENCY}$) is measured in RXC clock periods. The maximum latency is 81 RXC clock periods. If the latency is not an exact multiple of RXC clock periods, then the latency value is rounded down to the next lower number of RXC clock periods for the minimum latency and rounded up to the next higher integer number of RXC clock periods for the maximum latency. The standard requires a round-trip latency of less than 224 high-speed clock cycles.

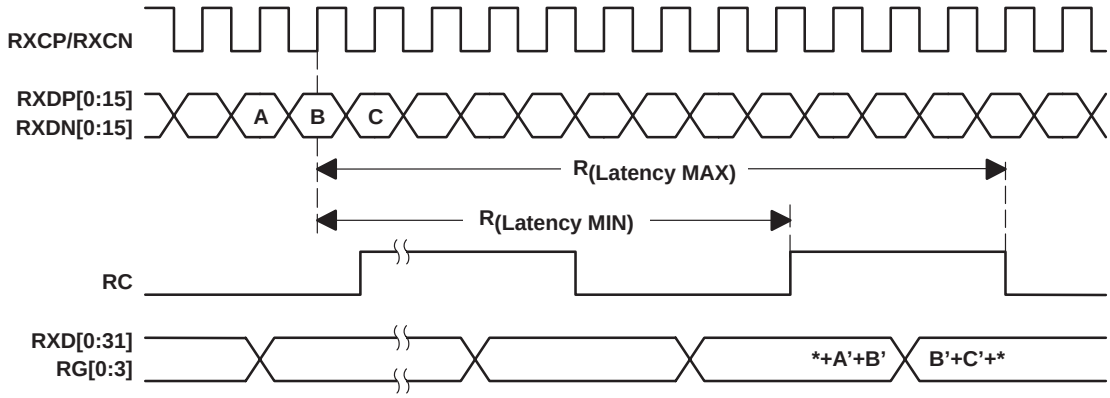


Figure 9. Receive Latency

detailed description (continued)

MDIO management interface

The DLKPC192S supports the management interface (MDIO) as defined in the IEEE 802.3-2000 Ethernet standard. (Note: This is not the same as defined in the IEEE 802.3ae standard, clause 45.) The DLKPC192S supports PCS registers as defined in this specification. At the time of definition of the DLKPC192S, the register set for PCS devices was in flux so a suitable definition was selected and implemented.

The MDIO interface allows register-based management and control. Normal operation of the device is possible without use of this interface because all of the essential signals necessary for operation are accessible via the device terminals. However, some additional features are accessible only through the MDIO.

The MDIO interface provides a means of external access to the registers within the DLKPC192S. Access is via two I/O signals: an input clock to the device and a bidirectional data signal. Commands and data are transferred one bit at a time by placing a bit value on the data line and clocking that bit using the clock line. Commands consist of two basic types: read and write. Except during a portion of a read command as described below, the data line is configured as an input to the DLKPC192S.

The MDIO interface is a daisy-chained interface and often connects multiple devices such as the DLKPC192S to a processor. The result is that other devices may reside on the MDIO bus that is connected to the DLKPC192S. Each command sent over the MDIO interface includes an address field that determines the device on the MDIO interface for which the command is intended. The DLKPC192S has five input terminals that determine its MDIO address (DVAD0 through DVAD4).

If no commands are being transferred, the data line is held in the high state with pullups to ensure a 1 is seen on the interface. The clock line can be continuously running or it may be idled (high or low) to conserve power and then restarted to transfer a new command, provided minimum pulse duration timings are maintained.

The MDIO management interface consists of a bidirectional data path (MDIO) and a clock reference (MDC). The protocol for reading from the internal registers is shown in Figure 10 The protocol for writing to the internal registers is shown in Figure 11. Detailed timing information is provided later in this document. The following paragraphs explain the two diagrams.

The sending device should send 32 or more consecutive 1s prior to beginning a new command. These 1s are known as the preamble. The DLKPC192S requires only two 1s between commands as command lengths are fixed.

A new command is indicated by sending 01 after the preamble. Code 01 is the start-of-frame indicator. After the start-of-frame indicator is the 2-bit command field. Code 10 is the command code for a read. Code 01 is the command code for a write. Codes 00 and 11 are invalid.

Immediately following the command code are 5 bits of device address. If the address matches the address assigned to the DLKPC192S then the command is processed by the DLKPC192S; otherwise the command is ignored, although it may be processed by another device on the MDIO interface.

Immediately following the address are 5 bits of register address. The register address specifies which of the possible 32 registers within the DLKPC192S is to be accessed (i.e., read or written based upon the command value). If the register address is that of a nonexistent DLKPC192S register, writes are ignored and reads are answered with zeros.

The two bit times following the register address are used as turnaround bits. These bits times are used for read operations, but exist even in write operations. During write operations, the sender sends a 10 sequence during these two bit times. During read operations, the sender stops driving the data signals during the first bit time and the addressed device starts driving a 0 during the second bit time. It should be noted that, while the data from the processor is valid on the rising edge of MDC, data from the device is clocked onto the MDIO signal using the rising edge. The timing of the data read during a read command has a different timing relationship to MDC than data being transferred by the processor.

MDIO management interface (continued)

Following the turnaround bits are 16 data bits. These are the values to be written to the addressed register during write commands, or they are the values read from the addressed register during read commands.

During the bit time after the last data bit, the data signal may be released and the pullup on the line will bring the data signal back to its idle state of all 1s.

Bit ordering is summarized in Table 1.

Table 1. MDIO Command Description

	PRE	ST	OP	PHY AD	REG AD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

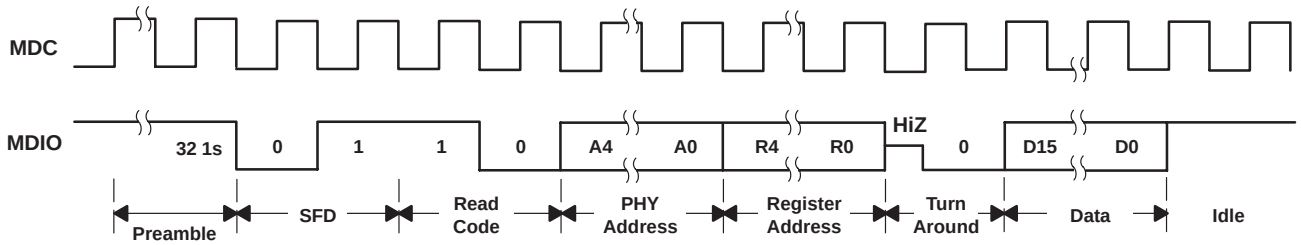


Figure 10. Management Interface Read Timing

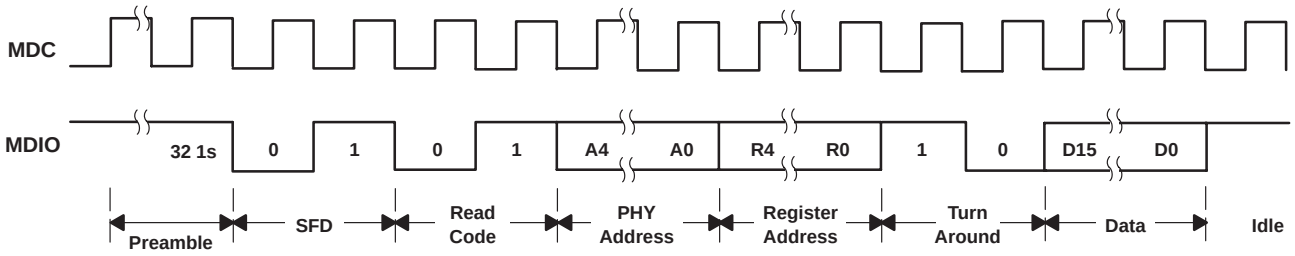


Figure 11. Management Interface Write Timing

The MDIO management interface allows up to 32 16-bit internal registers. Sixteen registers are reserved by the IEEE 802.3-2000 standard for definition and 16 are assigned for vendor-specific usage. The DLKPC192S implements five registers defined by the proposed IEEE 802.3ae standard and four vendor-specific registers. The IEEE-defined registers are listed in Table 2. The bit usage within these registers is defined in Table 3, Table 4, Table 5, and Table 6. The vendor-specific registers are defined in Table 7. The bit usage within these registers is defined in Table 8, Table 9, Table 10, and Table 11.

Table 2. MDIO Registers

REGISTER ADDRESS	REGISTER NAME	DEFINITION
0	Control	See Table 3
1	Status	See Table 4
2,3	PHY identifier	See Table 5
4−14	Not applicable	
15	Extended status	See Table 6

Table 3. Control Register Bit Definitions (Register 0)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
0.15	Reset	Logically ORed with the inverse of RSTN terminal 1 = Global resets including FIFO clear 0 = Normal operation When the reset bit is set to one, it automatically clears itself to zero upon completion of the reset function.	Read/write Self-clearing
0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode (default) When enabled, the transmit XSBI bus signals are internally routed to the receive XSBI bus signals. The transmit XSBI output terminals are held at zero and the receive XSBI input terminals are ignored when loopback is enabled. This mode requires the TXCP/N output clock to be connected to the RXCP/N input clock. The first few transitions of the RXCP/N clock are required for the device to come out of reset.	Read/write
0.13	Power Down	1 = Power-down mode is enabled. 0 = Normal operation (default) When enabled, all sections of the DLKPC192S, with the exception of the MDIO interface logic, are held reset and the internal clock distribution is disabled to minimize power usage. All inputs to the DLKPC192, except for those related to the MDIO interface, are ignored. All outputs remain driven, but are held at steady states. A reset is required after the part is subsequently powered back up.	Read/write
0.12:0	Reserved	Write as 0. Ignore on read	—

Table 4. Status Register Bit Definitions (Register 1)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
1.15:11		Read returns 10000b.	Read-only
1.10	PCS link status	1 = Link up when both the transmit path and receive path are functional 0 = Link down	Read-only
1.9	PCS high BER	1 = High BER. When 64b/66b receiver is detecting a BER > 10E−4. 0 = Low BER. When 64b/66b receiver is detecting a BER < 10E−4. Note, return of low indication requires 250 μs following high BER detection.	Read-only
1.8	PCS sync done	1 = PCS synchronized to received frames 0 = PCS not synchronized to received frames	Read-only
1.7:0	Reserved	Read returns 0	Read-only

Table 5. PHY Identifier Bit Defintions (Registers 2, 3)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
2.15:0	Bits 3:18 of the organizationally unique identifier (OUI) for Texas Instruments	Read returns 0x8000.	Read-only
3.15:10	Bits 19:24 of the OUI for Texas Instruments	Read returns 0x14.	Read-only
3.9:4	Model number	Read returns 0x04.	Read-only
3.3:0	Revision number	Read returns 0x0 (subject to change).	Read-only
(3.15:0)	Complete register value (informational)	Read returns 0x5040 (subject to change).	Read-only

Table 6. Extended Status Register Bit Defintions (Register 15)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15.15:12	Various configurations	Read returns 0	Read-only
15.11:0	Reserved	Read returns 0	Read-only

Table 7. Vendor Unique Registers

REGISTER ADDRESS	REGISTER NAME
16	Transmitter status
17	Receive status
18	TX and RX control
19	Test mode control
20−31	Reserved

Table 8. Transmitter Status Bit Definitions (Register 16)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
16.15	TXI_OVFL	Transmit FIFO has detected an overflow error. Event is latched to ensure observability.	Read-only Self-clearing
16.14	TXI_UNFL	Transmit FIFO has detected an underflow error. Event is latched to ensure observability.	Read-only Self-clearing
16.13	TXI_DEL	Transmit FIFO has detected movement toward overflow which should result in an automatic deletion. Event is latched to ensure observability. This is not an indication of an error.	Read-only Self-clearing
16.12	TXI_INS	Transmit FIFO has detected movement toward underflow which should result in an automatic insertion. Event is latched to ensure observability. This is not an indication of an error.	Read-only Self-clearing
16.11:10	Reserved	First read always returns 01. Subsequent reads are indeterminate.	Read-only Self-clearing
16.9:0	Reserved	Read returns 0.	Read-only

NOTE: Power-on reset value: 0x0400.

Table 9. Receiver Status Bit Definitioins (Register 17)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
17.15	RXO_OVFL	Receive FIFO has detected an overflow error. Event is latched to ensure observability.	Read-only Self-clearing
17.14	RXO_UNFL	Receive FIFO has detected an underflow error. Event is latched to ensure observability.	Read-only Self-clearing
17.13	RXO_DEL	Receive FIFO has detected movement toward overflow which should result in an automatic deletion. Event is latched to ensure observability. This is not an indication of an error.	Read-only Self-clearing
17.12	RXO_INS	Receive FIFO has detected movement toward underflow which should result in an automatic insertion. Event is latched to ensure observability. This is not an indication of an error.	Read-only Self-clearing
17.11:10	Reserved	First read always returns 01. Subsequent reads are indeterminate	Read-only Self-clearing
17.9	RXG_HIBER_SAV	64/66b bit error rate (BER > 10E−4). The occurrence of this condition does not cause the receive state machine to transition to the RX_INIT state and it does not output line fault characters on the XGMII receive interface.	Read-only Self-clearing
17.8:1	RXG_ERR_CNT	Frame-sync BER count. Contains the value from the most recent 250-µs count period. Changes automatically once every 250 µs	Read-only Self-clearing
17.0	Reserved	Read returns 0.	Read-only

NOTE: Power-on reset value: 0x0400.

Table 10. Transmitter and Receiver Control Bit Definitions (Register 18)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
18.15:10	MDIO_DEL_SPC[5:0]	Minimum number of deletable idle words that must be passed between deletion events. Default is 16.	Read/write
18.9	MDIO_RCNT_EBL	Transmission start up delay enable. Controls whether a minimum of eight idle words must be detected on the XGMII transmit path before the transmit path is enabled. Default is 1, enabled.	Read/write
18.8	MDIO_AKR_NI	Reads value from I/O terminal.	Read-only
18.7:0	Reserved	Read returns 0.	Read-only

NOTE: Power-on reset value (IDLE MODE): 0x4200.
Power-on reset value (AKR MODE): 0x4300.

Table 11. Test Mode Bit Definitions (Register 19)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
19.15:11	Reserved	Read returns 0.	Read-only
19.10	MDIO_RXC_BYPASS	Bypass receive decomposer	Read/write
19.9	MDIO_RXS_BYPASS	Bypass receive descrambler	Read/write
19.8	MDIO_TXC_BYPASS	Bypass transmit composer	Read/write
19.7	MDIO_TXS_BYPASS	Bypass transmit scrambler	Read/write
19.6:0	Reserved	These bits must be maintained at the default value of 0.	Read/write

NOTE: Power-on reset value: 0x0000.
These bits are intended for test only and should not be programmed to any value except 0x0000.

IPG modes

The XGMII interface transports information that consists of packets and interpacket gap (IPG) characters. While the proposed IEEE 802.3ae standard defines that the IPG, when transferred over the XGMII interface, consists of idle characters, industry practice has also defined a mode in which the IPG consists of other characters. This alternative mode character set is that used by XAUI devices to replace the idles within the IPG. This character set consists of alignment characters (A), control characters (K) and replacement characters (R).

The DLKPC192S can operate in one of two modes: AKR mode or idle mode. The configuration control terminal AKR_NI selects the mode.

In AKR mode, AKR_NI = 1, the DLKPC192S converts all AKR characters to idle characters, performs insertion or deletion on the idle characters, and transmits only encoded idle characters out the XSBI interface. The receive channel expects encoded idle characters to enter the XSBI, and performs insertions and deletions on idle characters only.

In idle mode, AKR_NI = 0, the DLKPC192S expects the IPG to consist of a sequence of idle characters on the XGMII interface and encoded idle characters on the XBSI interface. Both the transmit and receive FIFOs rely upon a valid idle stream to perform clock tolerance compensation.

In sumamry, if the system in which the DLKPC192S is placed presents AKR characters on the XGMII transmit input interface, the AKR_NI pin must be set high. If the system presents idle characters on the XGMII input, the AKR_NI pin must be set low. In both configurations, the device always outputs idle characters on the XGMII receive output interface and encoded idle characters on the XSBI transmit output interface. In addition, the device always requires encoded idle characters to be available on the XSBI receive input interface. Finally, the DLKPC192S is not able to perform clock tolerance compensation on local fault characters (LF) or remote fault characters (RF), so the IPG must contain some idle characters during these conditions.

detailed description (continued)

clocks

There are five interfaces on the DLKPC192S device: the XGMII transmit interface, the XGMII receive interface, the XSBI transmit interface, the XSBI receive interface, and the MDIO interface (see Figure 1).

The XGMII transmit and receive interfaces operate at the same frequency and are specified identically. While the clocks associated with the XGMII interface share specifications, the DLKPC192S places no requirement that these clocks operate at exactly the same rate or have any phase relationship to each other. TC is the transmit clock and is an input to the DLKPC192S. RC is the receive clock and is an output of the DLKPC192S. RC is generated from a reference clock, RFC, which is an input to the DLKPC192S. RFC is input using LVDS on terminals RFCP/RFCN. The two clock input signals associated with the XGMII transmit and receive interfaces, TC and RFC, are expected to run continuously.

The XSBI transmit and receive interfaces operate at the same frequency and are specified identically. While the clocks associated with the XSBI interface share specifications, the DLKPC192S places no requirement that these clocks operate at exactly the same rate or have any phase relationship to each other. RX is the receive clock and is an input to the DLKPC192S. TX is the transmit clock and is an output of the DLKPC192S. TX is generated from a reference clock, XBIC, which is an input to the DLKPC192S. XBIC is input using LVDS on terminals XBICP/XBICN. The two clock input signals associated with the XSBI transmit and receive interfaces, RX and XBIC, are expected to run continuously.

The MDIO interface uses a clock (MDC) to strobe data into or out of the DLKPC192S. While there are maximum frequency requirements for this clock, there is no minimum frequency. A system implementation, providing it meets all of the other requirements for the MDIO interface, need not provide a continuously running MDC clock signal.

power-on reset

The DLKPC192S uses an external power-on reset. Upon application of minimum valid power, power-on reset may be removed as required by the system. While the DLKPC192S is being held reset: the XGMII outputs, including the RC clock output are held low; the XSBI outputs are forced to toggle. Reset may be applied at anytime. It is recommended that when reset is asserted that reset be held for a minimum of 1 microsecond (after minimum valid power is applied). All clock inputs are expected to be valid at the time that reset is deasserted.

Shortly after a reset has occurred, the DLKPC192S begins outputting local fault and idle characters on the XGMII interface and properly encoded local fault and idle characters on the XSBI interface. The local fault characters are generated at the output of the FIFOs. For the transmit path, the local fault character must propagate through the DLKPC192S before it can appear on the XSBI output.

For the transmit path, local faults continue to be generated until:

1. At least eight valid idle or replacement character sets are transmitted to the DLKPC192S across the XGMII interface, at which time the XGMII data is routed to the transmit FIFO.
2. The transmit FIFO is filled to its midpoint (approximately 32 bytes or 8 XGMII transfers), at which time transferring of data out of the FIFO is enabled.
3. The data from the FIFO propagates through the 64b/66b encoder and the transmit gearbox and appears on the XSBI transmit bus.

For the receive path, local faults continue to be generated until:

1. Frame lock can be established using the input at the XSBI receive interface.
2. The data propagates through the 66b/64b decoder, through the receive FIFO and appears on the XGMII receive bus.

The MDIO interface accepts valid commands immediately following the deassertion of the reset signal.

detailed description (continued)

error handling

There are three types of errors that can be detected within the DLKPC192S. The three types are loss of frame synchronization, bit errors, and FIFO errors (overruns or underruns). Loss of frame synchronization can only occur on the receive path. Some, but not all, bit errors can be detected during the 64b/66b encode or decode process. FIFO errors can occur only if a clock on either the XGMII or XSBI is significantly out of specification or if there are insufficient and/or improper IPGs. If the clocks are within specification and a valid packet stream is being sent or received, FIFO errors do not occur. Reaction to each type of error is described in the following paragraphs.

The DLKPC192S resets frame synchronization at power-up or reset. Until frame synchronization is accomplished, the DLKPC192S outputs a local fault character on the receive XGMII bus. The link status is set to zero (link down) whenever the local fault character is being generated. Once frame synchronization is completed, the DLKPC192S can perform normal operations.

Bit errors typically occur on the receive path of the DLKPC192S but could also occur on the transmit path. Bit errors can be detected on the receive side either by detection of a framing error or by detection of an error during the 66b/64b decode process. Bit errors on the transmit path can only be detected during the 64b/66b encoding process. While the DLKPC192S device may detect some bit errors, many of the errors will likely go undetected as the functional definition of a PCS type device does not include a method for reliable detection. If a bit error is detected, the response by the DLKPC192S is to replace the received data containing the error with an encoded control value signifying that an error occurred. Basically, the corrupted data is replaced with defined error characters. If the rate of bit errors is high enough, frame synchronization could be lost. If frame synchronization is lost, the DLKPC192S begins generating local fault characters. Because frame synchronization is a function of the receive path and not the transmit path, local fault character generation as a result of bit errors can occur only on the receive path.

The FIFOs within the DLKPC192S are sufficient to handle differences in clock rates between the XGMII and the XSBI interfaces. Differences in clock rates are likely to occur, but only within specified limits. The depth of the DLKPC192S FIFOs, the maximum packet sizes and the minimum interpacket gaps (IPGs) specified by the Ethernet standards, along with the algorithms implemented within the DLKPC192S ensure that the FIFOs never underrun or overrun during normal operation. If there is a system malfunction that causes the inputs to the DLKPC192S to go out of specification, it is possible that the DLKPC192S could experience a FIFO underrun or overrun. If the DLKPC192S detects such a condition, it sets an error condition flag in the vendor specific registers, resets the link status, and generates local fault on the receive XGMII bus. The DLKPC192S must be reset (soft or hard) to clear this error condition.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . −0.5 V to 2.4 V
I/O supply voltage range: VDDS (see Note 1) . . . . . −0.5 V to 4 V
VDDO (see Note 1) . . . . . −0.5 V to 4 V
Voltage on any SSTL input terminal . . . . . −0.5 V to VDDO+0.5 V
Voltage on any SSTL output terminal . . . . . −0.5 V to VDDO+0.5 V
Voltage on any LVDS input terminal . . . . . −0.5 V to VDDS+0.5 V
Voltage on any LVDS output terminal . . . . . −0.5 V to VDDS+0.5 V
Voltage on any LVTTL input terminal . . . . . −0.5 V to VDDS+0.5 V
Voltage on any LVTTL output terminal . . . . . −0.5 V to VDDS+0.5 V
Electrostatic discharge (see Note 2) . . . . . Class 3, A:2 kV
Case temperature under bias . . . . . −55°C to 125°C
Junction temperature under bias . . . . . −55°C to 150°C
Storage temperature . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminals.
2. This rating is measured using MIL-STD-883C Method, 3015.7.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	1.71	1.8	1.89	V
I/O supply voltage, VDDS	3.135	3.3	3.465	V
I/O supply voltage, VDDO	2.375	2.5	2.625	V
Operating free-air temperature, T_A	0		70	°C

supply voltage power dissipation

	TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{DD} supply voltage power dissipation, $P_{D,VDD}$	C_L = 15 pF, a5 pattern used			510	mW
VDDS I/O supply voltage power dissipation, $P_{D,VDDS}$				400	
VDDO I/O supply voltage power dissipation, $P_{D,VDDO}$				580	

LVDS I/O characteristics

LVDS electrical characteristics free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_I	Input voltage		0		2	V
V_O	Output voltage	V_{REF} = 1.2 V, R_{bias} = 1 kΩ, R_L = 50 Ω	0.925		1.475	V
V_{ID}	Input differential voltage		0.1			V
R_{bias}	Current bias reference resistor			1k		Ω
R_I	Input differential impedance	On-chip termination	80	100	120	Ω
R_O	Output differential impedance	On-chip termination	80	100	120	Ω
V_{REF}	Reference voltage		1.14	1.2	1.26	V
$\|V_{OD}\|$	Differential steady-state output voltage magnitude	R_L = 50 Ω	250		400	mV
I_{IH}	LVDS high-level input current	V_{IH} = VCC			−11	μA
I_{IL}	LVDS low-level input current	V_{IL} = 0 V			−30	μA
C_I	Input capacitance			0.34		pF
C_O	Output capacitance			5.17		pF

† All typical values are at T_A= 25°C and with V_{DDS} = 3.3 V.

LVDS driver switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Differential output signal rise time (10% to 90%)	R_L = 100 Ω, C_L = 10 pF	0		0.5	ns
t_f	Differential output signal fall time (90% to 10%)		0		0.5	ns

SSTL I/O DC characteristics

SSTL electrical characteristics free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage for input buffers		−0.3		V_{DDO}+0.3	V
V_O	Output voltage for output buffers		0		V_{DDO}	V
V_{OH}	High-level output voltage		V_{REF}+0.38			V
V_{OL}	Low-level output voltage				V_{REF}−0.38	V
V_{IH}	High-level input voltage		V_{REFH}+0.18			V
V_{IL}	Low-level input voltage				V_{REFH}−0.18	V
C_I	Input capacitance				1.73	pF
V_{REF}	Reference voltge		$0.5 \times V_{DDO}$			V

SSTL driver switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time (10% to 90%)	R_L = 50 Ω, C_L = 10 pF, 40-Ω series terminator at source	0		0.5	ns
t_f	Differential output signal fall time (90% to 10%)		0		0.5	ns

LVTTL I/O DC characteristics

LVTTL electrical characteristics free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage for input buffers		−0.3		V_{DDO}+0.3	V
V_O	Output voltage for output buffers		0		V_{DDS}	V
V_{OH}	High-level output voltage		2.4			V
V_{OL}	Low-level output voltage				0.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
C_I	Input capacitance				1.57	pF

LVTTL driver switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_r	Output signal rise time (10% to 90%)	R_L = 50 Ω		7.9	0.5	ns
t_f	Differential output signal fall time (90% to 10%)			7.8	0.5	ns

† All typical values are at T_A= 25°C and with V_{DDS} = 3.3 V.

timing—reference clocks

RFC clock requirements

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f, frequency	Maximum data rate	TYP−0.01%	156.25	TYP+0.01%	MHz
Frequency tolerance		−100		100	ppm
Duty cycle		45%	50%	55%	
Jitter, peak-to-peak				40	ps

XBIC clock requirements

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f, frequency	Maximum data rate	TYP−0.01%	644.53125	TYP+0.01%	MHz
Frequency tolerance		−100		100	ppm
Duty cycle		45%	50%	55%	
Jitter, peak-to-peak				40	ps

A note on timing diagrams:

The IEEE standard defines the data-valid levels between 20% and 80% of the maximum voltage. On the XSBI interface, with realistic rise and fall times specified and met at 400 ps for both the data and clock, this would leave no margin onT_{CQ_PRE} and T_{CQ_POST} for the following variables: data-to-data matching (16 lines), clock-to-data matching, process variation, temperature variation, voltage variation, jitter sources internal and external. This specification is not possible to meet given this definition. Additionally, the ASIC design tools currently on the market report all timing parameters at the 50% points. Also, LVDS cells typically latch very close to the 50% points making a larger data-invalid window unnecessary. For these reasons, timing specifications in the following four sections are interpreted for data valid at the 50% crossing points.

XSBI

The XSBI transmit interface timings are detailed in Table 12 and shown in Figure 12.

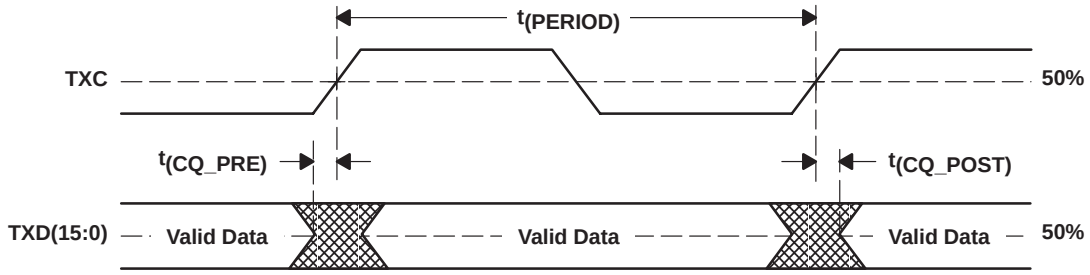


Figure 12. XSBI Transmit Timing Diagram

Table 12. XSBI Transmit AC Specification

PARAMETER		MIN	TYP	MAX	UNIT
$t_{(PERIOD)}$	PMA_TX_CLK period for LAN operation	1.551360	1.551515	1.551670	ns
$t_{(CQ\_PRE)}$	Data-invalid window prior to TXC			200	ps
$t_{(CQ\_POST)}$	Data-invalid window after TXC			200	ps
$t_{(DUTY)}$	PMA_TX_CLK duty cycle	40%		60%	

NOTE: Minimum data-invalid window with respect to TXC

XSBI (continued)

The XSBI receive interface timings are detailed in Table 13, and shown in Figure 13. Note, the phase relationship is such that the positive side of the differential clock needs to rise *in the middle of the data*. This is in contrast to the transmit XSBI interface. On that interface, the positive side to the clock is in phase with the data. To successfully loop the transmit path to the receive path of this PCS device you must attach TXCP to RXCN and TXCN to RXCP.

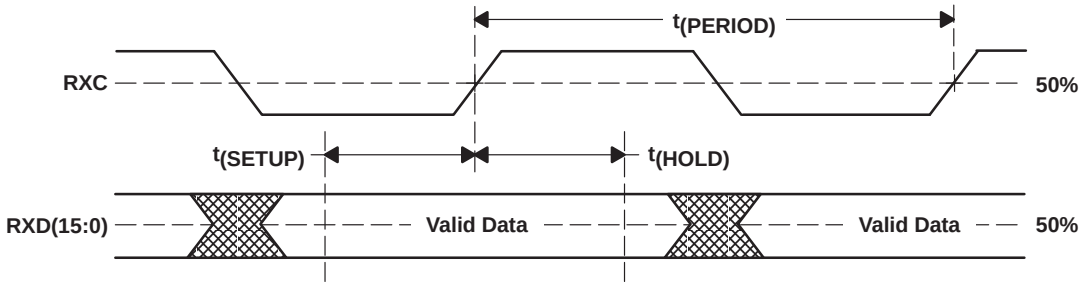


Figure 13. XSBI Receive Timing Diagram

Table 13. XSBI Receive Timing

PARAMETER		MIN	TYP	MAX	UNIT
$t_{(PERIOD)}$	PMA_RX_CLK period		1.551515		ns
$t_{(DUTY)}$	PMA_RX_CLK duty cycle	45%		55%	
$t_{(SETUP)}$	Data-setup before RXC	300			ps
$t_{(HOLD)}$	Data-hold after RXC	300			ps

XGMII

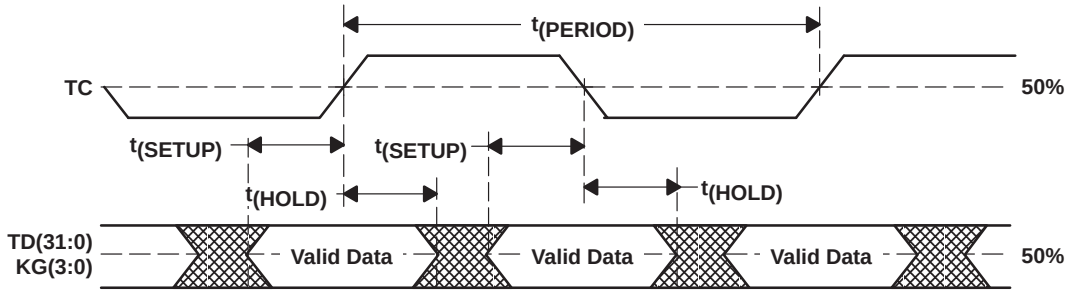


Figure 14. XGMII Transmit Timing Diagram

Table 14. XGMII Transmit AC Specification

PARAMETER		MIN	TYP	MAX	UNIT
$t_{(PERIOD)}$	TC transmit clock (received by DLKPC192S)		6.4		ns
$t_{(SETUP)}$	Data-setup to rising or falling edge of TC	480			ps
$t_{(HOLD)}$	Data-hold from rising or falling edge of TC	480			ps
$t_{(DUTY)}$	TC duty cycle	40%		60%	

XGMII (continued)

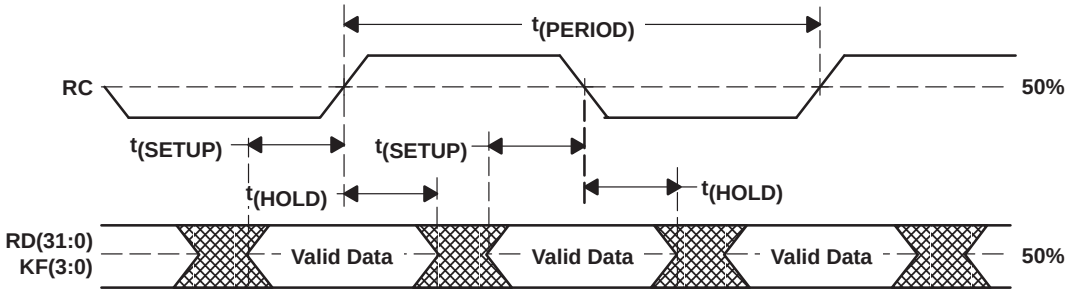


Figure 15. XGMII Receive Timing Diagram

Table 15. XGMII Receive AC Specification

PARAMETER		MIN	TYP	MAX	UNIT
$t_{(PERIOD)}$	RC receive clock (received by DLKPC192S)		6.4		ns
$t_{(SETUP)}$	Data-setup to rising or falling edge of RC	650†			ps
$t_{(HOLD)}$	Data-hold from rising or falling edge of RC	960			ps
$t_{(DUTY)}$	RC duty cycle	40%		60%	

† RD5, RD9, RD10, and RD11 do not meet the IEEE specification of 960 ps, RD5 being the worst channel with the least setup time. There exists excess hold margin, the minimum hold time being 1.3 ns, to allow for board-level clock delay to meet the IEEE 960-ns setup-time requirement.

MDIO

The technology and timing for the MDIO interface was under flux within the 802.3ae task force during the definition of the DLKPC192S. In the DLKPC192S, the MDIO interface technology was chosen to be LVTTL.

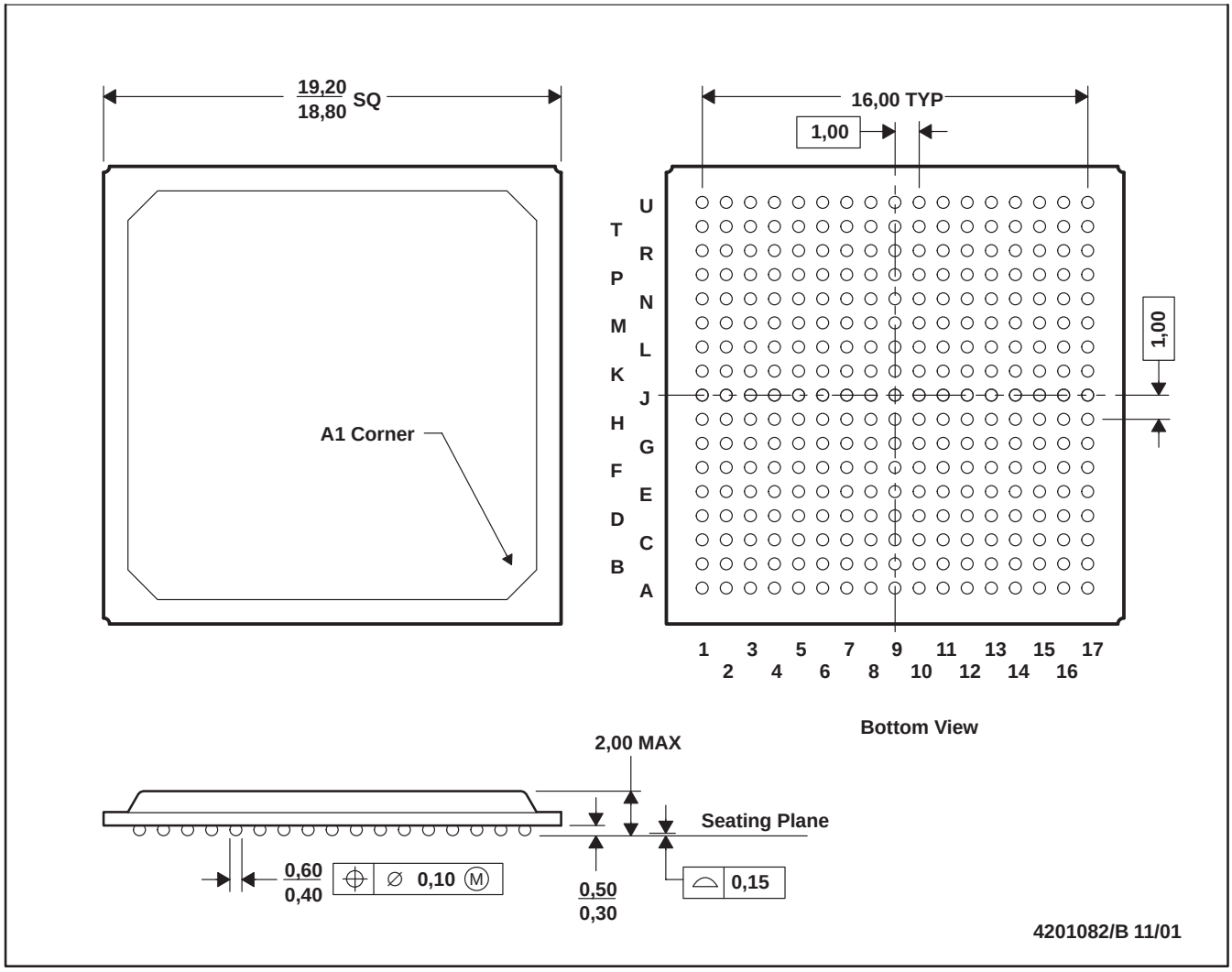
testability

Test functionality was added to the DLKPC192S to support device evaluation and test during manufacturing. This functionality is intended for use by Texas Instruments. The TEST input signal, if set to 1, enables various test modes. When TEST is true, some of the input and output signals of the DLKPC192S may change functionality.

While harm to the device is not likely to occur if TEST modes are enabled, users of the DLKPC192S are advised to tie the TEST terminal to 0 at all times.

MECHANICAL DATA

GNT (S-PBGA-N289) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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